



Dediprog On-Board Programming

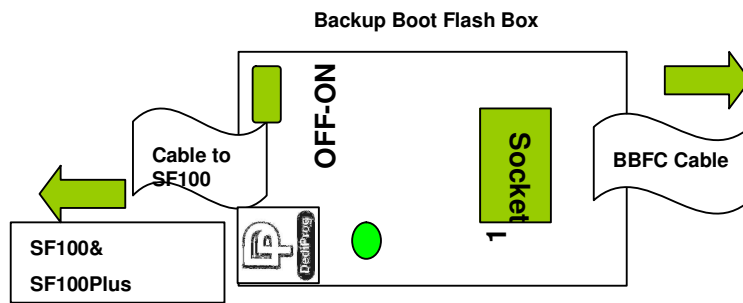
DEFAULT PIN & Cable Assignment

Dediprog SF100 & SF100 Plus Programmer PIN Assignment (top view)

1	I/O1	I/O4	2
3	I/O2	Vdd	4
5	Vcc	GND	6
7	CS	CLK	8
9	MISO	MOSI	10
11	Vpp	I/O3	12
13	SCL	SDA	14

Pin	Signal	Description
1, 2, 3, 12	General I/O	General I/O are used to control optional pins of the memory (hold, Wp) or switch the application in specific mode (reset Chipset or switch OFF MOSFET)
4	Vdd	Vdd is used to supply the programmer with 5V from the application to work in Stand alone mode.
5	Vcc	Vcc is used to supply the application memory
6	GND	GND is the common ground shared between application and programmer
7	CS	SPI Chip select of the Application memory
8	CLK	SPI clock signal for the application memory
9	MISO	Data out from the Application memory: MISO
10	MOSI	Data In of the Application memory: MOSI
11	Vpp	High voltage applied on the memory to speed up the operation
13, 14	SCL, SDA	I2C bus for future purpose

Backup Boot Flash Kit with 2X5 Pin header to the application

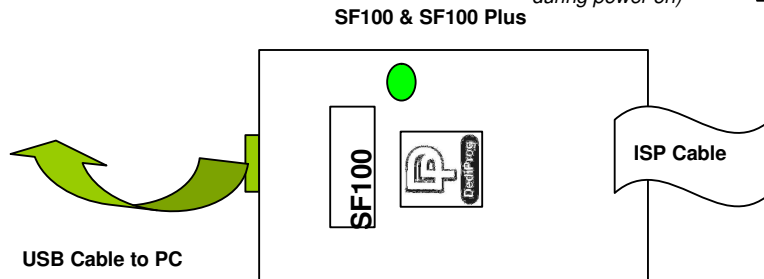


Application system (top view)

Cs2 is used only in dual-serial flash platform

1	none	CS2	2
3	CS1	Vcc	4
5	MISO	Hold	6
7	Not used	CLK	8
9	GND	MOSI	10

SF100 & SF100 Plus with 2x4 Pin header to the application
(for application system with isolation on spi bus during power off or chipset SPI in high impedance during power on)



Application system (top view)

Red Wire: Vcc

1	Vcc	GND	2
3	CS	CLK	4
5	MISO	MOSI	6
7	Vpp	I/O3	8

WARNING: mistake proof pin

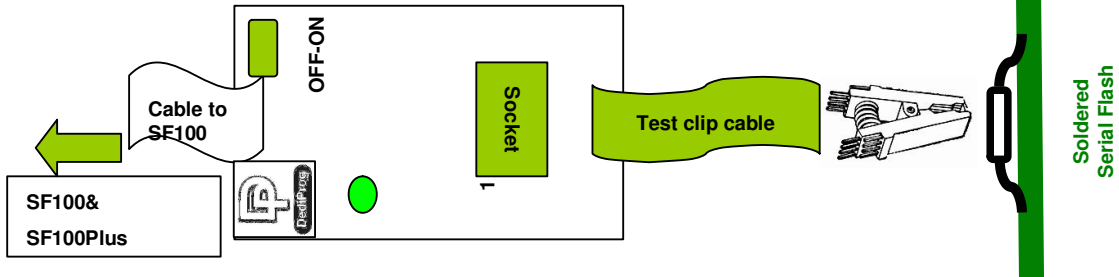
Customers have to put mistake proof pin In order to avoid wrong insertion which may result in the malfunction of the programmer or the application system pin header

Method: remove an unused pin of the pin header on the application system and insert the pin or glue in the corresponding hole of the pin header connecting to the cable



Dediprogram On-Board Programming DEFAULT PIN & Cable Assignment

Backup Boot Flash Kit with Test Clip to the application
Backup Boot Flash Box



Locate Pin 1 on the test clip. Connect the test clip directly to the soldered serial flash on board

SF100 & Sf100 Plus with Test Clip to the application
(for application system with isolation on spi bus during power off or chipset SPI in high impedance during power on)

SF100 & SF100 Plus

